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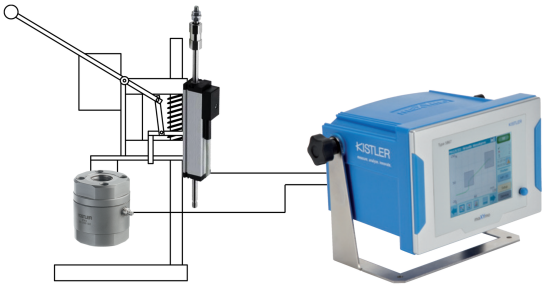
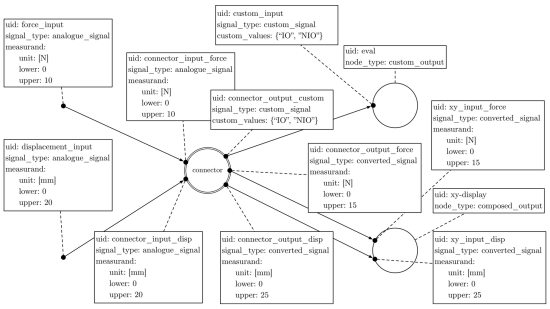
Development of a Modelling Procedure for the Description of Test Set-Ups with Measuring Instruments

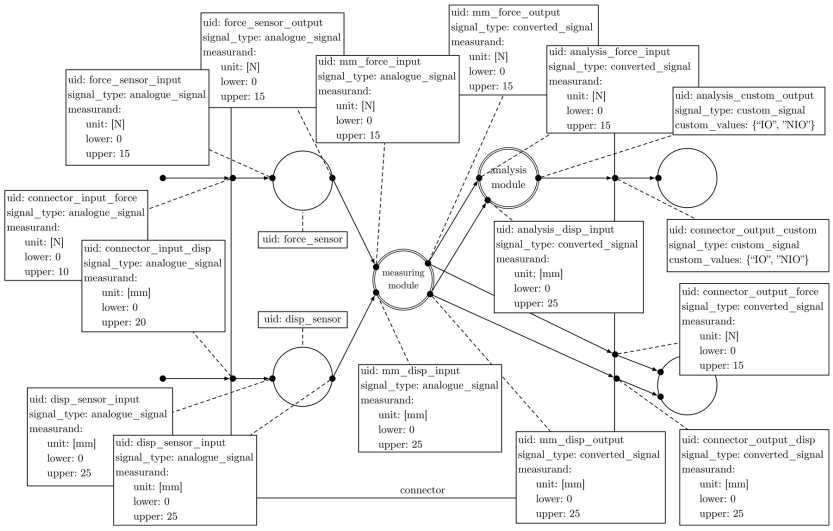
A formal language for modelling and verifying test set-ups



Exemplary Test Set-Up



Abstraction Level 1: Defining Inputs & Outputs



Abstraction Level 2: Defining Sensors & Modules

Problem: Measurement techniques are a highly complex field in which small technical details decide over the accuracy and therefore the success or failure of a measurement. What sensors can be used? How can noise be handled properly? These and many more are questions one has to answer when wanting to capture the measurand of interest.

Modelling a test set-up requires experience and is therefore mostly done by experts in the field. The lack of uniform modelling approaches makes this difficult. Discussing models can lead to confusion when a common language is missing. Furthermore, the verification of a model on different abstraction levels has to be done manually since the necessary tool support is missing. This manual verification is error-prone.

Solution: This thesis provides a common formal language for describing test set-ups. It does so by proposing a modelling approach for test set-ups which allows the definition of different abstraction levels on top of a general set of rules. These rules allow the verification of the set-up. For example, it can be verified if components are configured correctly. This was achieved by defining a set of verification constraints in first-order logic. These constraints are then applied to a graph representing the test set-up. A formal specification of the model and its verification is provided and backed by an implementation in the language Prolog.