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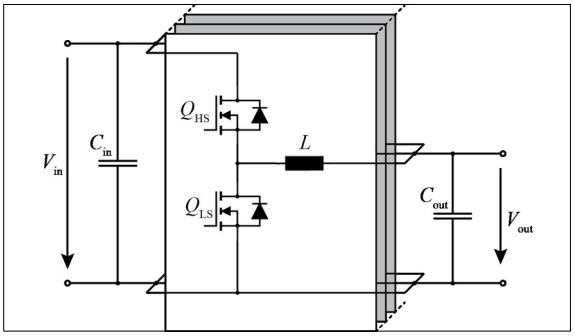
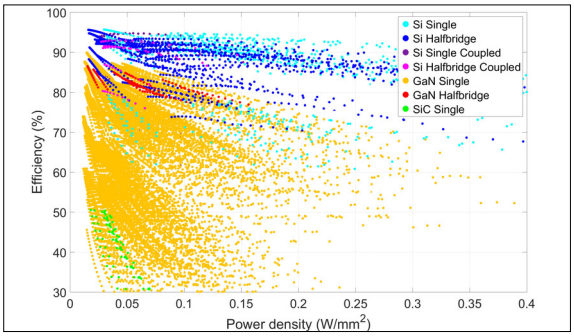
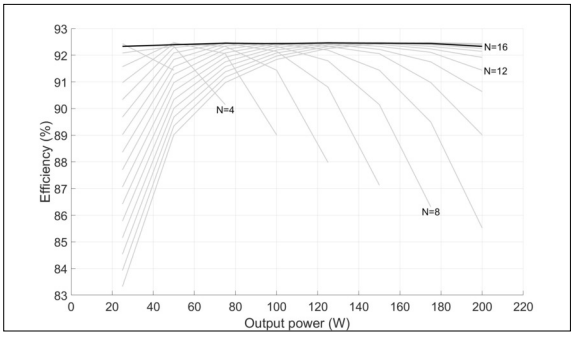
Design of a Programmable Power Supply for IBM's Microserver



Proposed interleaved synchronous buck converter.



Power density for MOSFET technologies. 'Single' are two separate MOSFETs whereas 'Halfbridge' is one combined component.



Phase shedding (black) enables to select the best possible operation point within different number of phases (grey).

Introduction: Data centers constitute around 2 % of the global energy consumption with an ascending trend. To limit this growth of demand, IBM introduced 2015 its Microserver concept in order to increase computational throughput per unit volume. This can be accomplished by stacking nodes each containing a microprocessor and memory close to each other. IBM's concept does not only increase computational efficiency but it also enables the possibility of Big-Data applications like the DOME/SKA project where a large data center consisting of Microservers will be used for processing 14 Exabyte of raw sample-data and archiving at a rate of 1 Petabyte per day (1 Exabyte = 1'000 Petabyte = 1'000'000 Terabyte). A dense stacking of the nodes causes a high power demand at low voltage and high currents. To achieve an acceptable efficiency, which is vital for an overall high computational efficiency, all power supplies must be located as close to the nodes as possible in order to reduce copper losses to a minimum.

Objective: Currently used 12-1 VDC converters operate at about 80 % efficiency at full load. On every node is one step-down converter supplied by a 'thermal-power copper plane'. In addition one Power Supply board delivers power used by the node's RAM. The goal is to design and test a programmable power supply chain for 12-1 VDC and possibly 48-1 VDC step-down conversion which always performs at its peak efficiency irrespective of load change. Exploration of a limited set of down conversion topologies, such as half/full-bridge buck converter or multi-level fly capacitor converter, is required. Available off-the-shelf power MOSFETs based on Si, GaN or SiC technologies and available inductors, non-coupled or coupled, are being used for converter designs. In order to perform at high efficiency over a large load range the power stages are parallelized in branches and phase shedding is applied, meaning number of phases can dynamically be changed to achieve better efficiency at variable operating conditions. An independent Programmable Power Supply Array (PPSA) with a maximum output power of 200 W and different topologies is to be built. The optimal number of phases is investigated in term of available space and overall efficiency. Controlled by a microcontroller/FPGA the PPSA should always perform at maximum possible efficiency for different loads.

Result: Due to low conduction losses in the inductors and semiconductors and the low number and size of active and passive components the half-bridge converter is evaluated as the topology with the highest efficiency potential. Therefore, the half-bridge converter, in particular an interleaved synchronous buck converter, is the targeted and focused solution. The functionality of the phase shedding method can be demonstrated using simulations. The optimal number of phases can be up to 18, however, in order to limit designing effort this number is kept to a maximum of 16. Because of low voltage currents are extremely high. Thus, conduction losses in semiconductors are as important as switching losses. The test PPSA is focused on a 12-1 VDC conversion build by silicon 'Halfbridge' MOSFETs. Theoretically, this converter achieves an overall efficiency of maximum 92.4 %. Since this test PPSA is currently being fabricated no measurements can be presented at this time.