

Introduction

This document describes the specifications for the General Purpose Input/Output (GPIO) core for the On Chip Processor Bus (OPB). The OPB GPIO is a 32-bit peripheral that attaches to the OPB.

Features

- OPB v2.0 bus interface with byte-enable support
- Configurable as single or dual GPIO channel(s)
- Number of GPIO bits configurable from 1 to 32 bits
- Each GPIO bit dynamically programmable as input or output
- Can be configured as inputs-only on a per channel basis to reduce resource utilization
- Ports for both 3-state and non 3-state connections
- Independent reset values for each bit of all registers
- Optional interrupt request generation

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	QPro™-R Virtex™-II, QPro Virtex-II, Spartan™-II, Spartan-II-E, Spartan-3, Spartan-3E, Virtex, Virtex-II, Virtex-II Pro, Virtex-4, Virtex-E, and Virtex-5	
Version of Core	opb_gpio	v3.01b
Resources Used (GPIO_WIDTH = 32)		
	Min	Max
Slices	See Table 12 and Table 13	
LUTs		
FFs		
Block RAMs	N/A	N/A
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE 8.2i or later	
Verification	ModelSim SE/EE 6.0 or later	
Simulation	ModelSim SE/EE 6.0 or later	
Synthesis	XST 8.2i or later	
Support		
Support provided by Xilinx, Inc.		

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Functional Description

The OPB GPIO design provides a general purpose input/output interface to a 32-bit On-Chip Peripheral Bus (OPB). The OPB GPIO can be configured as either a single or a dual channel device. The channel width is configurable and when both channels are enabled, the channel width remains the same for both.

The OPB GPIO design supports 3-state, as well as independent input and output, ports. An input port may be configured to take its external input either from the bidirectional 3-state pin or from the dedicated input only pins. For a port configured as output, the data is driven out through a 3-state buffer as well as to an output-only pin. The ports can be configured dynamically for input or output by enabling or disabling the 3-state buffer.

Each channel is individually configurable as input ports only. When a channel is configured as input-only, the logic required to implement the output path and the three-state controls are removed resulting in reduced resource utilization.

The channels may be configured to generate an interrupt when a transition on any of their inputs occurs.

The major interfaces and modules of the design are shown in **Figure 1** and described in the subsequent sections. The OPB GPIO design is comprised of the OPB_IPIF and the GPIO_CORE modules.

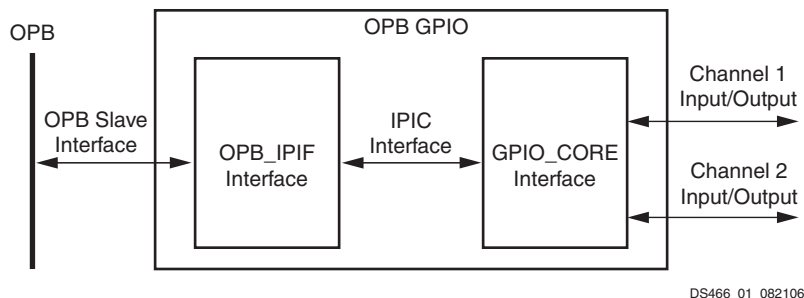


Figure 1: OPB GPIO Block Diagram

OPB_IPIF

OPB_IPIF provides an interface between GPIO_CORE and the OPB 32-bit bus standard. It supports the following functions:

- OPB slave interface: The OPB_IPIF module implements the basic functionality of OPB slave operation and does the necessary protocol and timing translation between the OPB and the IPIC interface
- Interrupt support: The OPB_IPIF module provides support for enabling interrupts, to capture an interrupt event, and to maintain the interrupt status. The registers required to support interrupts are implemented within this module.

For more information on OPB_IPIF interface, see the OPB IPIF documents listed in the **Reference Documents** section of this document.

GPIO_CORE

GPIO_CORE provides an interface between the IPIC interface and the OPB GPIO channels. The GPIO_CORE consists of registers and multiplexers for reading and writing the OPB GPIO channel

registers. It also includes the necessary logic to identify an interrupt event when the channel input changes.

Figure 2 shows a detailed diagram of dual channel implementation of the GPIO_CORE. The 3-state buffers in the figure are not actually part of the core. The 3-state buffers are added in the synthesis process, usually automatically with an Add I/Os option. For the sake of simplicity, the control signals of the IPIC interface are not shown in Figure 2.

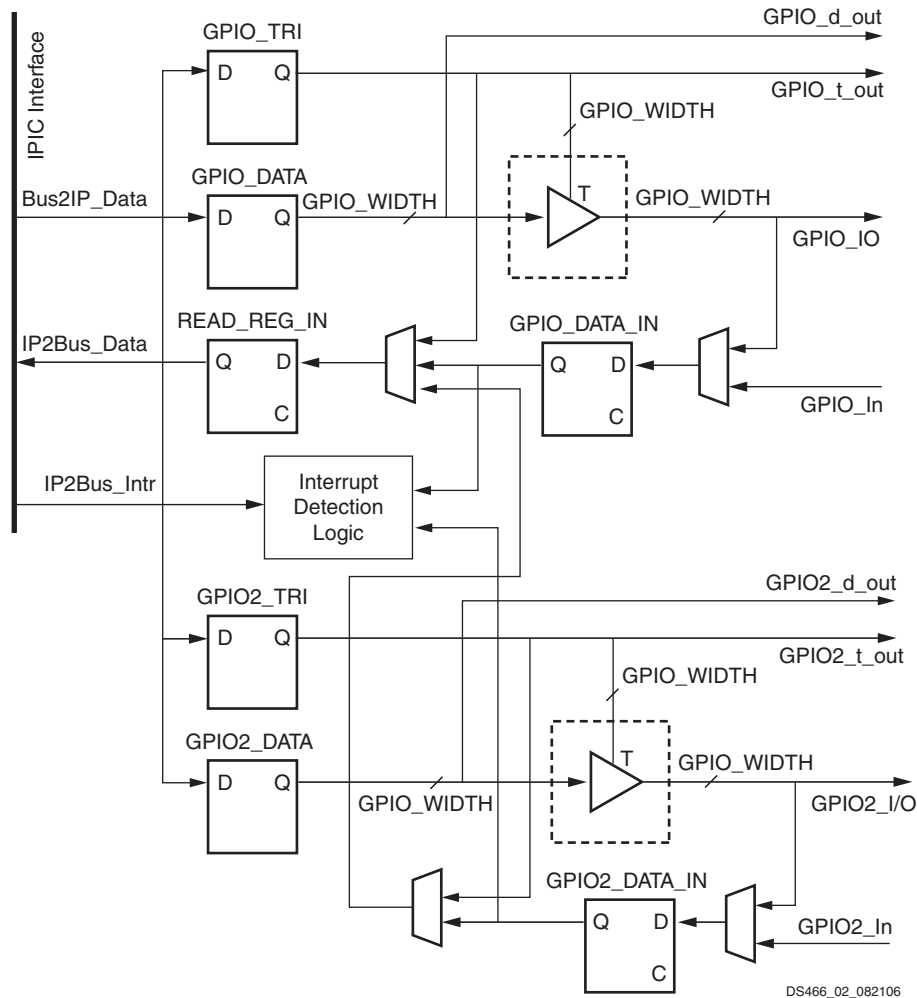


Figure 2: GPIO_CORE Dual Channel Implementation

OPB GPIO Design Parameters

Certain features can be parameterized in the OPB GPIO design. Some of these parameters control the interface to the OPB while others provide information to tailor the GPIO_CORE logic to minimize resource utilization. The features that can be parameterized in the OPB GPIO are shown in Table 1.

Table 1: OPB GPIO Design Parameters

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
GPIO					
G1	OPB GPIO Base Address	C_BASEADDR	Valid OPB Address (1,2)	None (3)	std_logic_vector
G2	OPB GPIO High Address	C_HIGHADDR	Valid OPB Address (1,2)	None (3)	std_logic_vector
G3	Target FPGA Family	C_FAMILY	Any FPGA family	virtex2	string
G4	GPIO Data Bus Width	C_GPIO_WIDTH	1-32	32	integer
G5	OPB GPIO Interrupt	C_INTERRUPT_PRESENT	0/1	0	integer
G6	Inputs Only	C_ALL_INPUTS	0/1	0	integer
G7	Select GPIO_IO as input source	C_IS_BIDIR	0/1	1	integer
G8	GPIO_DATA reset value	C_DOUT_DEFAULT	Any valid std_logic_vector	00000000	std_logic_vector
G9	GPIO_TRI reset value	C_TRI_DEFAULT	Any valid std_logic_vector	FFFFFFFF	std_logic_vector
G10	Use dual channel	C_IS_DUAL	0/1	0	integer
G11	Channel 2 inputs only	C_ALL_INPUTS_2	0/1	0	integer
G12	Channel 2 select GPIO_IO as input source	C_IS_BIDIR_2	0/1	1	integer
G13	GPIO2_DATA reset value	C_DOUT_DEFAULT_2	Any valid std_logic_vector	00000000	std_logic_vector
G14	GPIO2_TRI reset value	C_TRI_DEFAULT_2	Any valid std_logic_vector	FFFFFFFF	std_logic_vector
G15	User ID for MIR / reset register	C_USER_ID_CODE	0-255	3	integer
OPB Interface					
G16	OPB Address Width	C_OPB_AWIDTH	32	32	integer
G17	OPB Data Width	C_OPB_DWIDTH	32	32	integer

Notes:

1. The range specified by C_BASEADDR and C_HIGHADDR must comprise a complete, contiguous power of two range such that the range = 2^n and the n least significant bits of C_BASEADDR is zero. This range needs to encompass the address range required by the OPB GPIO
2. The minimum address range specified by C_BASEADDR and C_HIGHADDR must be at least 0xFF
3. No default value will be specified to ensure that the actual value is set i.e. if the value is not set, a compiler error will be generated

Allowable Parameter Combinations

The range specified by C_BASEADDR and C_HIGHADDR must encompass the memory space required by the OPB GPIO. The minimum range specified by C_BASEADDR and C_HIGHADDR should be at least 0xFF. If C_INTERRUPT_PRESENT parameter is set then the address range specified by C_BASEADDR and C_HIGHADDR should be at least 0x1FF.

No default value will be specified for C_BASEADDR and C_HIIGHADDR in order to enforce that the user configures these parameters with the actual values. If the values are not set for C_BASEADDR and C_HIGHADDR, a compiler error will be generated.

OPB GPIO I/O Signals

The I/O signals for this reference design are listed in [Table 2](#).

Table 2: OPB GPIO I/O Signals

Port	Signal Name	Interface	I/O	Initial State	Description
OPB					
P1	OPB_ABus(0:C_OPB_AWIDTH-1)	OPB	I		OPB Address Bus
P2	OPB_BE(0:C_OPB_DWIDTH/8-1)	OPB	I		OPB Byte Enables
P3	OPB_DBus(0:C_OPB_DWIDTH-1)	OPB	I		OPB Data Bus
P4	OPB_RNW	OPB	I		OPB Read, Not Write
P5	OPB_select	OPB	I		OPB Select
P6	OPB_seqAddr	OPB	I		OPB Sequential Address
P7	SIn_DBus(0:C_OPB_DWIDTH-1)	OPB	O	0	OPB GPIO Data Bus
P8	SIn_errAck	OPB	O	0	OPB GPIO Error Acknowledge
P9	SIn_retry	OPB	O	0	OPB GPIO Retry (Always inactive)
P10	SIn_toutSup	OPB	O	0	OPB GPIO Timeout Suppress (Always inactive)
P11	SIn_xferAck	OPB	O	0	OPB GPIO Transfer Acknowledge (Always inactive)
System					
P12	OPB_Clk	OPB	I		OPB Clock
P13	OPB_Rst	OPB	I		OPB Reset
P14	IP2INTC_Irpt	IPIF Interrupt	O	0	OPB GPIO Interrupt Active high signal
P15	GPIO_in(0 to C_GPIO_WIDTH-1)	GPIO	I		Channel 1 General purpose input
P16	GPIO_d_out(0 to C_GPIO_WIDTH-1)	GPIO	O	0 ⁽¹⁾	Channel 1 data register (GPIO_DATA) output
P17	GPIO_t_out(0 to C_GPIO_WIDTH-1)	GPIO	O	1 ⁽²⁾	Channel 1 3-state control register (GPIO_TRI) output
P18	GPIO_IO(0 to C_GPIO_WIDTH-1)	GPIO	I/O	Z ⁽³⁾	Channel 1 General purpose I/O

Table 2: OPB GPIO I/O Signals (Contd)

Port	Signal Name	Interface	I/O	Initial State	Description
P19	GPIO2_in(0 to C_GPIO_WIDTH-1)	GPIO	I		Channel 2 General purpose input
P20	GPIO2_d_out(0 to C_GPIO_WIDTH-1)	GPIO	O	0 ⁽⁴⁾	Channel 2 data register (GPIO2_DATA) output
P21	GPIO2_t_out(0 to C_GPIO_WIDTH-1)	GPIO	O	1 ⁽⁵⁾	Channel 2 3-state control register (GPIO2_TRI) output
P22	GPIO_IO(0 to C_GPIO_WIDTH-1)	GPIO	I/O	Z ⁽⁶⁾	Channel 2 General purpose I/O

Notes:

1. GPIO_d_out has an initial value of 0 only if the default value of C_DOUT_DEFAULT is used.
2. GPIO_t_out has an initial value of 1 only if the default value of C_TRI_DEFAULT is used.
3. GPIO remains at high impedance only if the default value of C_TRI_DEFAULT is used.
4. GPIO2_d_out has an initial value of 0 only if the default value of C_DOUT_DEFAULT_2 is used.
5. GPIO2_t_out has an initial value of 1 only if the default value of C_TRI_DEFAULT_2 is used.
6. GPIO2 remains at high impedance only if the default value of C_TRI_DEFAULT_2 is used.

Parameter - Port Dependencies

The width of the OPB GPIO channel registers depends on some of the parameters. In addition, when certain features are parameterized away, the related logic is removed. The dependencies between the OPB GPIO design parameters and the I/O ports are shown in [Table 3](#).

Table 3: Parameter-Port Dependencies

Name	Affects	Depends	Relationship Description
C_OPB_DWIDTH	OPB_BE OPB_DBus SIn_DBus	0 to (C_OPB_DWIDTH/8) - 1 0 to C_OPB_DWIDTH - 1 0 to C_OPB_DWIDTH - 1	Number of byte enables decoded Width of the OPB data bus Width of the slave read data bus
C_OPB_AWIDTH	OPB_ABus	0 to C_OPB_AWIDTH - 1	Width of the OPB address bus
C_GPIO_WIDTH	GPIO_DATA GPIO_TRI GPIO2_DATA GPIO2_TRI	1 to C_GPIO_WIDTH	The size of the registers GPIO_DATA and GPIO_TRI determines the number of GPIO_in, GPIO_IO, GPIO_d_out and GPIO_t_out pins. Similarly, the size of the registers GPIO2_DATA and GPIO2_TRI determines the number of GPIO2_in, GPIO2_IO, GPIO2_d_out and GPIO2_t_out pins
C_IS_DUAL	GPIO2_in GPIO2_IO GPIO2_d_out GPIO2_t_out	1 to C_GPIO_WIDTH	When C_IS_DUAL is 1, channel 2 is created.
C_ALL_INPUTS	GPIO_IO GPIO_d_out GPIO_t_out	1 to C_GPIO_WIDTH	Eliminates the logic required for GPIO_d_out and GPIO_t_out. Both GPIO_d_out and GPIO_t_out are driven low. GPIO_IO ports are driven to high impedance

Table 3: Parameter-Port Dependencies (Contd)

Name	Affects	Depends	Relationship Description
C_ALL_INPUTS_2	GPIO2_IO GPIO2_d_out GPIO2_t_out	1 to C_GPIO_WIDTH	Eliminates the logic required for GPIO2_d_out and GPIO2_t_out. Both GPIO2_d_out and GPIO2_t_out are driven low. GPIO2_IO ports are driven to high impedance
C_IS_BIDIR	GPIO_IO GPIO_in	1 to C_GPIO_WIDTH	GPIO_IO is used for input rather than GPIO_in
C_IS_BIDIR_2	GPIO2_IO GPIO2_in	1 to C_GPIO_WIDTH	GPIO2_IO is used for input rather than GPIO2_in

OPB GPIO Registers

There are four internal registers in the OPB GPIO design as shown in [Table 4](#). These registers are implemented in the GPIO_CORE interface module. The memory map of the OPB GPIO design is determined by setting the C_BASEADDR parameter. The internal registers of the OPB GPIO are at a fixed offset from the base address. The OPB GPIO internal registers and their offset are listed in [Table 4](#).

Table 4: OPB GPIO Registers

Register Name	Description	OPB Address	Access
GPIO_DATA	Channel 1 OPB GPIO Data Register	C_BASEADDR + 0x00	Read/Write
GPIO_TRI	Channel 1 OPB GPIO 3-state Register	C_BASEADDR + 0x04	Read/Write
GPIO2_DATA	Channel 2 OPB GPIO Data register	C_BASEADDR + 0x08	Read/Write
GPIO2_TRI	Channel 2 OPB GPIO 3-state Register	C_BASEADDR + 0x0C	Read/Write

Depending on the value of certain configuration parameters, some of these registers are removed. The parameter - register dependency is described in [Table 5](#). A write to an unimplimented register has no effect. An attempt to read the unimplimented register will return unknown values.

Table 5: Parameter-Register Dependency

Parameter Values			Register Retainability			
C_IS_DUAL	C_ALL_INPUTS	C_ALL_INPUTS_2	GPIO_DATA	GPIO_TRI	GPIO2_DATA	GPIO2_TRI
0	1	X ⁽¹⁾	Yes	No	No	No
0	0	X ⁽¹⁾	Yes	Yes	No	No
0	1	X ⁽¹⁾	Yes	No	No	No
0	0	X ⁽¹⁾	Yes	Yes	No	No
1	1	1	Yes	No	Yes	No

Table 5: Parameter-Register Dependency (Contd)

Parameter Values			Register Retainability			
C_IS_DUAL	C_ALL_INPUTS	C_ALL_INPUTS_2	GPIO_DATA	GPIO_TRI	GPIO2_DATA	GPIO2_TRI
1	0	1	Yes	Yes	Yes	No
1	1	0	Yes	No	Yes	Yes
1	0	0	Yes	Yes	Yes	Yes
1	1	1	Yes	No	Yes	No
1	0	1	Yes	Yes	Yes	No
1	1	0	Yes	No	Yes	Yes
1	0	0	Yes	Yes	Yes	Yes

Notes:

1. When C_IS_DUAL = 0, the core is configured for single channel and hence the parameter C_ALL_INPUTS_2 has no effect
2. Depending on the value of C_GPIO_WIDTH, the data registers and the 3-state control registers (GPIO_DATA, GPIO_TRI, GPIO2_DATA and GPIO2_TRI) when implemented, get trimmed to the size of value specified by C_GPIO_WIDTH

OPB GPIO Data Register (GPIOx_DATA)

OPB GPIO data register is used to read the input ports and write to the output ports. When a port is configured as input, writing to the port has no effect. When a port is configured as output, reading the port returns the value of the corresponding bit in the OPB GPIO data register.

There are two OPB GPIO data registers (GPIO_DATA and GPIO2_DATA), one corresponding to each channel. The channel 1 data register (GPIO_DATA) is always present while the channel 2 data register (GPIO2_DATA) is present only if the core is configured for dual channel i.e. C_IS_DUAL = 1.

The OPB GPIO Data Register is shown in Figure 3 and Table 6 details its functionality.



Figure 3: OPB GPIO Data Register

Table 6: OPB GPIO Data Register Description

Bits	Name	Core Access	Description	Reset Value
0:31	GPIOx_DATA	Read/Write	OPB GPIO Data For I/O Programmed as inputs: R : Reads value on input pin W : No effect For I/O Programmed as outputs: R : Reads value in OPB GPIO data register W : Writes value to OPB GPIO data register and output pin	C_DOUT_DEFAULT C_DOUT_DEFAULT_2

OPB GPIO 3-State Register (GPIOx_TRI)

The OPB GPIO 3-state register is used to configure the ports dynamically as input or output. When a bit within this register is set, the corresponding I/O port is configured as input port. When a bit is reset, the corresponding I/O port is configured as output port.

There are two OPB GPIO 3-state control registers (GPIO_TRI and GPIO2_TRI), one corresponding to each channel. The channel 1 3-state control register (GPIO_TRI) is present when channel 1 is not configured for all input ports (C_ALL_INPUTS = 0). The channel 2 3-state control register (GPIO2_TRI) is present only if the core is configured for dual channel (C_IS_DUAL = 1) and channel 2 is not configured for all input ports (C_ALL_INPUTS_2 = 0).

The OPB GPIO 3-state Register is shown in Figure 4 and its functionality is described in Table 7.



DS466_04_110105

Figure 4: OPB GPIO 3-State Register

Table 7: OPB GPIO 3-State Register Description

Bits	Name	Core Access	Description	Reset Value
0:31	GPIOx_TRI	Read/Write	OPB GPIO 3-state control. Each I/O pin of the OPB GPIO is individually programmable as an input or output. For each bit: 0 I/O pin configured as output 1 I/O pin configured as input	C_TRI_DEFAULT C_TRI_DEFAULT_2

OPB GPIO Interrupts

The OPB GPIO can be configured under the control of the C_INTERRUPT_PRESENT generic to generate an interrupt when a transition occurs in any of the channel inputs. The GPIO_CORE interface module includes interrupt detection logic to identify any transition on channel inputs. When a transition is detected, the same is indicated to the OPB_IPIF module interface. The OPB_IPIF module implements the necessary registers to enable and maintain the status of the interrupts.

To support interrupt capability for channels, the OPB_IPIF interface module implements the following registers:

- OPB Global Interrupt Enable register (OPB GIE)
- IP Interrupt Enable Register (IP IER)
- IP Interrupt Status Register (IP ISR)

The IP IER implements independent interrupt enable bit for each channel while the OPB Global Interrupt Enable Register provides the master enable/disable for the interrupt output to the processor. The IP ISR implements independent interrupt status bit for each channel. The IP ISR provides Read and Toggle-On-Write access. The Toggle-On-Write mechanism for the IP Interrupt Status Register avoids the requirement on the user interrupt service routine to perform Read-Modify-Write operation to clear the status bit of the interrupt. Read-Modify-Write operations can lead to inadvertent clearing of interrupts captured in the time period between the read and write operations.

Table 8 details the OPB GPIO interrupt registers and their offset from the base address of OPB GPIO memory map. These registers are meaningful only if the C_INTERRUPT_PRESENT generic is set to 1.

Table 8: OPB GPIO Interrupt Registers

Register Name	Description	OPB Address	Access
OPB GIE	OPB Global Interrupt Enable Register	C_BASEADDR + 0x11C	Read/Write
IP IER	IP Interrupt Enable Register	C_BASEADDR + 0x128	Read/Write
IP ISR	IP Interrupt Status Register	C_BASEADDR + 0x120	Read/TOW[1]

Notes:

1. Toggle-On-Write (TOW) access toggles the status of the bit when a value of "1" is written to the corresponding bit

OPB Global Interrupt Enable Register (OPB GIE)

The OPB Global Interrupt Enable Register provides the master enable/disable for the interrupt output to the processor. This is a single bit read/write register as shown in Figure 5. This register is meaningful only if the parameter C_INTERRUPT_PRESENT is 1.

Note that this bit must be set to generate interrupts, even if the interrupts are enabled in the IP Interrupt Enable Register (IP IER). The bit definition for OPB Global Interrupt Enable Register is given in Table 9.



Figure 5: OPB Global Interrupt Enable Register

Table 9: OPB Global Interrupt Enable Register Description

Bit(s)	Name	Core Access	Reset Value	Description
0	Global Interrupt Enable	Read/Write	0	Master enable for the device interrupt output to the system interrupt controller. <ul style="list-style-type: none"> • 1 = Enabled • 0 = Disabled
1 - 31	Unused	N/A	0	Unused. Set to zeros on a read.

IP Interrupt Enable (IP IER) and IP Status Registers (IP ISR)

The IP Interrupt Enable Register (IP IER) and IP Interrupt Status Register (IP ISR), shown in Figure 6, provide a bit per interrupt. These registers are meaningful only if the parameter C_INTERRUPT_PRESENT is 1.

The interrupt enable bits in the IP Interrupt Enable Register have a one-to-one correspondence with the status bits in the IP Interrupt Status Register. The interrupt events are registered in the IP Interrupt Status Register by the OPB clock and therefore the change in the input port must be stable for at least one clock period wide to guarantee interrupt capture. Each IP ISR register bit can be set or cleared via software by the Toggle-On-Write implementation.

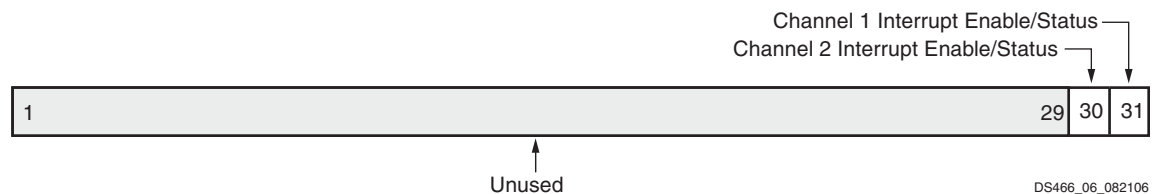


Figure 6: IP Interrupt Enable and IP Interrupt Status Register

The bit definition for IP Interrupt Enable Register and IP Interrupt Status Register are given in Table 10 and Table 11 respectively.

Table 10: IP Interrupt Enable Register Description

Bit(s)	Name	Core Access	Reset Value	Description
0 - 29	Unused	N/A	0	Unused. Set to zeros on a read.
30	Channel 2 Interrupt Enable	Read/Write	0	Enable Channel 2 Interrupt <ul style="list-style-type: none"> • 1 = Enabled • 0 = Disabled (masked)
31	Channel 1 Interrupt Enable	Read/Write	0	Enable Channel 1 Interrupt <ul style="list-style-type: none"> • 1 = Enabled • 0 = Disabled (masked)

Table 11: IP Interrupt Status Register Description

Bit(s)	Name	Core Access	Reset Value	Description
0 - 29	Unused	N/A	0	Unused. Set to zeros on a read.
30	Channel 2 Interrupt Status	Read/TOW ⁽¹⁾	0	Channel 2 Interrupt Status <ul style="list-style-type: none"> • 1 = Channel 2 input interrupt • 0 = No Channel 2 input interrupt
31	Channel 1 Interrupt Status	Read/TOW ⁽¹⁾	0	Channel 1 Interrupt Status <ul style="list-style-type: none"> • 1 = Channel 1 input interrupt • 0 = No Channel 1 input interrupt
Notes:				
1. Toggle-On-Write (TOW) access toggles the status of the bit when a value of 1 is written to the corresponding bit				

OPB GPIO Operation

The OPB GPIO can be configured as either a single or a dual channel device using the C_IS_DUAL generic. When both channels are enabled with C_IS_DUAL, each channel has the same size, as defined by the C_GPIO_WIDTH size.

The OPB GPIO has a 3-state I/O capability as well as independent inputs and outputs. This allows connection to both bi-directional and conventional signals. The GPIOx_TRI register is used to enable the 3-state buffers which enable/3-state outputs on the GPIOx_IO pins. The GPIOx_TRI register is also driven out of the dedicated GPIOx_t_out output pins. Each of the GPIOx_IO pin has a corresponding bit in the GPIOx_TRI register.

To configure a port as output, the corresponding bit in GPIOx_TRI register is written as 0. A subsequent write to the GPIOx_DATA register causes the data written to appear on the GPIOx_IO pins for I/Os that are configured as outputs. Data written to the GPIOx_DATA register is also driven out of the GPIOx_d_out output-only pins for non 3-state connections.

To configure a port as input, the corresponding bit in GPIOx_TRI register is written as 1 thereby disabling the 3-state buffers. An input port can be configured under control of the C_IS_BIDIRx generics, to take its external input from the bi-directional (GPIOx_IO) pins or the dedicated input only (GPIOx_in) pins. If C_IS_BIDIRx is 1, the source for inputs is the GPIOx_IO ports. If C_IS_BIDIRx is 0, the source for inputs is the GPIOx_in ports.

If only inputs are required for a channel, the C_ALL_INPUTSx parameter can be set to true. As a result, the GPIOx_TRI register and the read multiplexer are removed from the logic to reduce resource utilization. The related I/O pins (GPIOx_IO, GPIOx_d_out and the GPIOx_t_out) will be retained in the design and will be driven with the default value.

The GPIOx_DATA and the GPIOx_TRI registers are reset to the values set on the generics C_DOUT_DEFAULTx and C_TRI_DEFAULTx at configuration time.

If the C_INTERRUPT_PRESENT generic is 1, a transition on any input will cause an interrupt. There are independent interrupt enable and interrupt status bit for each channel if dual channel operation is used.

User Application Hints

The user may find the following steps helpful in accessing the OPB GPIO core:

For input ports when the channel is configured for interrupt

1. Configure the port as input by writing the corresponding bit in GPIOx_TRI register with the value of 1.
2. Enable the channel interrupt by setting the corresponding bit in the IP Interrupt Enable Register; Also enable the OPB Global Interrupt Enable Register by setting bit 0.
3. When an interrupt is received, read the corresponding bit in GPIOx_DATA register. Toggle the status in the IP Interrupt Status Register by writing the corresponding bit with the value of "1".

For input ports when the channel is not configured for interrupt

1. Configure the port as input by writing the corresponding bit in GPIOx_TRI register with the value of 1.
2. Read the corresponding bit in GPIOx_DATA register.

For output ports

1. Configure the port as output by writing the corresponding bit in GPIOx_TRI register with a value of 0.
2. Write the corresponding bit in GPIOx_DATA register.

OPB GPIO Timing Diagrams

This section shows the timing diagrams for the register read and write accesses to the OPB GPIO core.

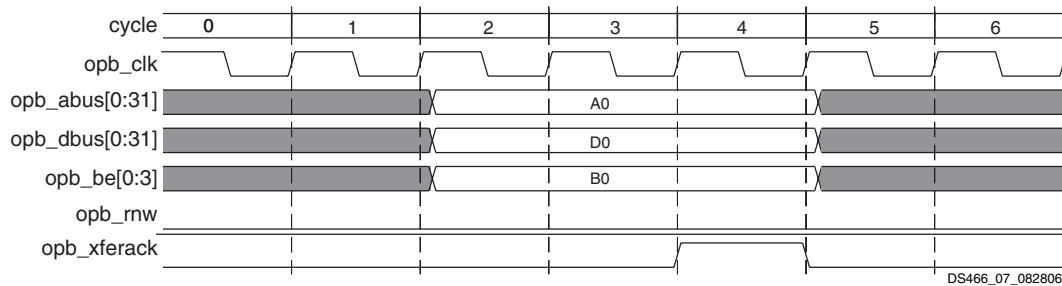


Figure 7: OPB GPIO Register Write

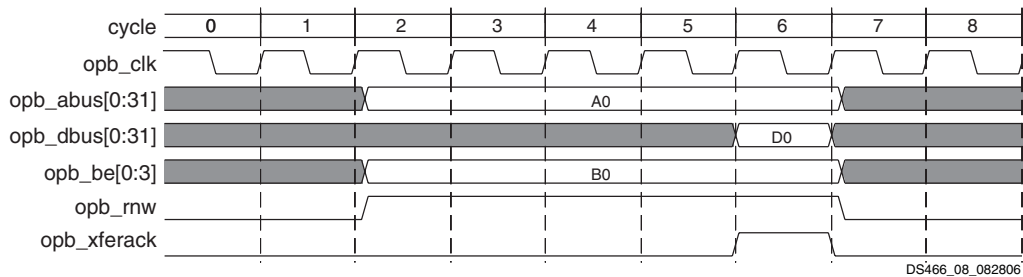


Figure 8: OPB GPIO Register Read

Design Implementation

Target Technology

The intended target technology is the Virtex-4 FPGA.

Device Utilization and Performance Benchmarks

Because the OPB GPIO module will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates. When the OPB GPIO module is combined with other designs, the utilization of FPGA resources and timing of the OPB GPIO design will vary.

The OPB GPIO benchmarks and the resource utilization for various parameter combinations are detailed in Table 12 and Table 13. Resource utilization is measured with Virtex-4 (xc4vlx25-10-ff668) and Virtex-5 (xc5vlx50-1-ff1153) as the target devices.

Table 12: Performance and Resource Utilization Benchmarks For Virtex-4 (xc4vlx25-10-ff668)

Parameter Values				Device Resources			F _{MAX} (MHz)
C_IS_DUAL	C_INTERRUPT_PRESENT	C_ALL_INPUTS	C_ALL_INPUTS_2	Slices	Slice Flip-Flops	LUTs	
0	0	1	X ¹	77	124	61	268.962
0	0	0	X ¹	135	224	197	304.878
0	1	1	X ¹	117	175	124	211.864
0	1	0	X ¹	168	270	193	205.973
1	0	1	1	100	159	102	322.061
1	0	0	1	182	275	230	300.210
1	0	0	0	222	343	230	229.463
1	1	1	1	157	242	302	219.829

Notes:

1. When C_IS_DUAL = 0, the core is configured for single channel and hence the parameter C_ALL_INPUTS_2 has no effect
2. These benchmark designs contain only the OPB GPIO module without any additional logic. Benchmark numbers approach the performance ceiling rather than representing performance under typical user condition
3. C_GPIO_WIDTH is set to 32 for all cases

Table 13: Performance and Resource Utilization Benchmarks For Virtex-5 (xc5vlx50-1-ff1153)

Parameter Values				Device Resources		F _{MAX} (MHz)
C_IS_DUAL	C_INTERRUPT_PRESENT	C_ALL_INPUTS	C_ALL_INPUTS_2	Slice Flip-Flops	LUTs	
0	0	1	X ¹	124	63	409.668
0	0	0	X ¹	227	163	352.485
0	1	1	X ¹	176	125	288.684
0	1	0	X ¹	271	222	258.532
1	0	1	1	162	96	371.195
1	0	0	1	257	136	298.597
1	0	0	0	257	136	373.832
1	1	1	1	327	175	282.247

Notes:

- When C_IS_DUAL = 0, the core is configured for single channel and hence the parameter C_ALL_INPUTS_2 has no effect
- These benchmark designs contain only the OPB GPIO module without any additional logic. Benchmark numbers approach the performance ceiling rather than representing performance under typical user condition
- C_GPIO_WIDTH is set to 32 for all cases

Reference Documents

The following documents contain useful information about the OPB GPIO reference design:

- *On-Chip Peripheral Bus Architectural Specifications, Version 2.0*, IBM
- *DS404 OPB IPIF Product Specification (v3.01.a)*, Xilinx

Revision History

Date	Version	Revision
12/1/03	1.0	Initial Xilinx release.
11/1/05	1.1	Converted to new DS template; updated figures to graphic standards; reformatted tables; made minor content edits.
12/1/05	1.2	Added Spartan-3E support.
5/15/06	1.3	Added Virtex-5 support.
8/29/06	1.4	Incorporated CR304158; updated figures, edited tables and content, updated legal footer.