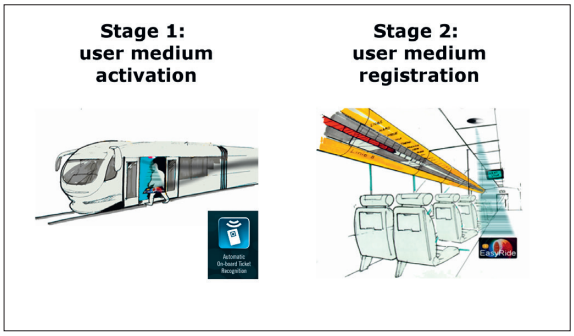
Simon Kuster

Nicola Ochsenbein

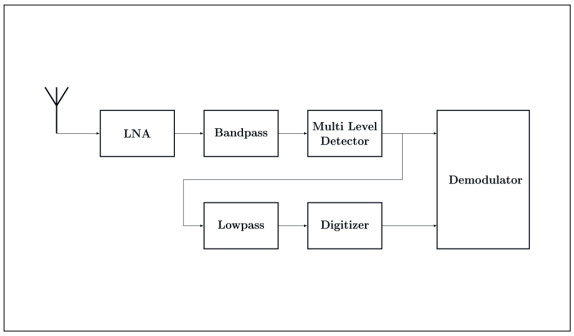
Graduate Candidates	Simon Kuster, Nicola Ochsenbein
Examiner	Prof. Dr. Paul Zbinden
Co-Examiner	Robert Reutemann, Miromico AG, Zürich, ZH
Subject Area	Mikroelektronik
Project Partner	Albis Technologies AG, Zürich, ZH

Nano-power low-frequency Receiver

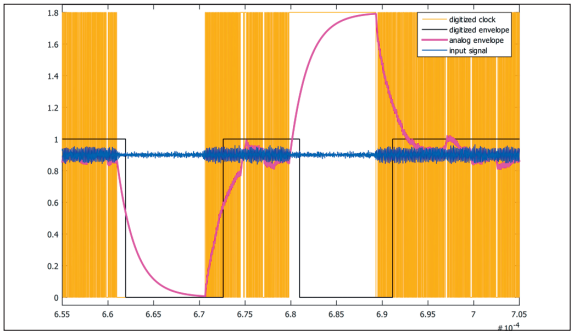
Development of a system design for a nano-power receiver, the corresponding high-level simulation model and implementation of a comparator and demodulator



Be-In/Be-Out: two phase registration process



System block design of the front-end of the first stage



Simulated analog and digital output signals of the front-end of the first stage

Introduction: The BeIn-BeOut ticketing system, developed by Albis Technologies Ltd., was designed on behalf of SBB as a functional model and is certified. Without the need for user interaction, the battery-powered user medium is registered during the journey, using a cryptographic wireless communication channel. In the background, the system evaluates the best price and each customer receives an individual bill. With this solution, also non-frequent travelers benefit from the comfort of a season ticket. The user medium should have the size of a credit card and a life time of 3 years. The part that most influences power consumption is the first stage. It is the most frequently active part, and it detects whether the user has entered a public transport vehicle or not. The development of this first stage is the challenge of this bachelor thesis. Beside the development of the system design and the simulation model, the partial implementation of the first stage, including analog and digital electronics, is part of this project.

Approach/Technologies: These days numerous papers can be found about low-power receivers. Most of them operate at much higher frequencies. Therefore, these systems are not of interest for the present project. Different high-level system designs were developed and discussed with Albis Technologies Ltd. Specifications for each block had been evaluated and tested with simulations to build the system. Some of the specifications could be adapted from the previous chip version.

Result: The main product of this work is the system design. The simulation model is built with Matlab/Simulink. The receiver chain is grouped in blocks, which represent functional parts. The specifications for each block of the system design can be evaluated with this simulation model. The complete system model can be used to verify the functionality of the receiver chain. It is user-friendly to change the input parameters, tolerances and absolute values to check new design options. The secondary product is the implementation of system parts. In the analog domain, the digitizer is implemented as a one bit ADC. In the digital part, the demodulator is implemented. It decodes the incoming signal into a bit stream, which will be sent to the telegram detector for further processing. The digitizer is implemented with Tanner S-Edit on schematic level. The demodulator is realized as a VHDL model. Based on the implementation results of the digitizer it is expected that the specifications for the power consumption can be met.