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Subject Area	Mobilkommunikation
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Digital IQ demodulator based on two-channel FPGA-based digitiser

Phase noise measurement

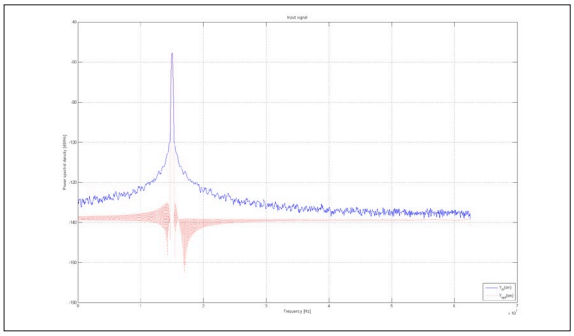

Illustration 1: Phase noised sinusoid. Red clean reference signal. Blue phase noised signal

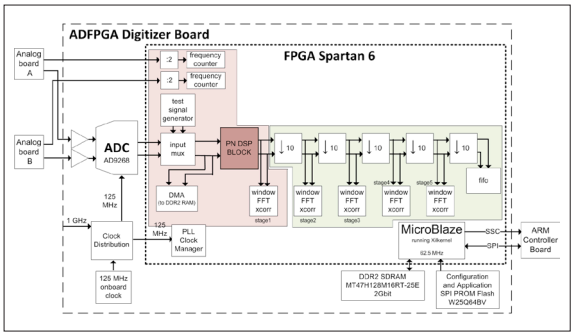

Illustration 2: Simplified visualisation of the multistage FFT with the phase noise digital signal processing block marked in red

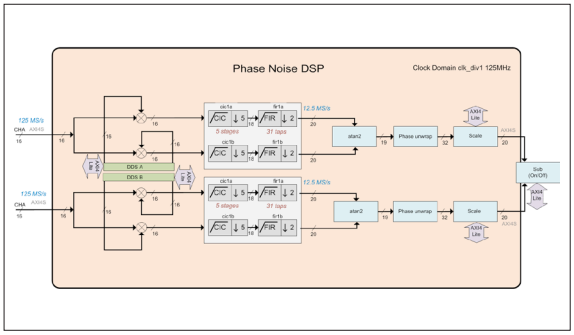

Illustration 3: Detailed visualisation of the phase noise digital signal processing implementation

Introduction: A real oscillator produces a sinusoidal signal that can contain phase noise. Phase noise can be modelled as $A\sin(\omega t + \varphi(t))$ where $\varphi(t)$ represents normally distributed white noise. Due to this, its PSD exhibits power at frequencies other than the wanted carrier frequency which makes the oscillation of the generated sinusoid unclean. Illustration 1 shows a phase noised sample sinusoid (blue) and a clean reference sinusoid (red).

Objective: The goal is to visualise the phase noise spectral density in [dBV^2] at [Hz] offset from the carrier. The setup to expand is a board hosting two differential, analogue input sockets. The input signals are digitised via a 125 MS/s A/D converter. The digitised input signal is then further processed through an FFT implementation using a Xilinx Spartan 6 FPGA. A multistage FFT and a very precise frequency counter have already been implemented before this thesis by Patrick Fleischmann (ICOM) using Xilinx Design Suite. Illustration 2 shows the concept and the position of the phase noise DSP.

Solution: The two-channel phase noise DSP is visualised in illustration 3. A digital I/Q mixer is used to separate the real and imaginary part of the input signal and downmodulate it to baseband. After low-pass filtering both, an implementation of atan2 is used to recover the phase information of the input signal. Atan2 is a 4-quadrant version of the arctan function, which means it is defined in all 4 quadrants of the coordinate system. However 2π or -2π phase jumps occur on every transition between two quadrants. This effect can visually be described as phase wrapping into a $[-\pi, \pi]$ domain. A phase unwrapper has therefore been implemented using the concept of a finite state machine. Furthermore a direct digital synthesiser (DDS) cannot be set to the input frequency with infinite precision. Also the input frequency may vary over time due to temperature or other non-ideal effects on the oscillator device under test (DUT). Due to the use of phase unwrapping and DDS instead of a PLL, adjustments to long-time frequency deviations of the DUT are not possible. An increasing discrepancy between the DDS and the DUT frequencies introduces a slope that superimposes itself on the real phase course. Since HW registers have a maximal representable number, a linear scale block has been implemented to prevent overflow of the output HW registers. In the end, the two input channels are subtracted from one another to minimise phase jitter created by the A/D conversion.