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Subject Area	Sensor, Actuator and Communication Systems
Project Partner	Dr. Fritz Faulhaber GmbH & Co. KG, D - Schönaich

Advanced Hall Sensor

Backend Design, Test & Specification

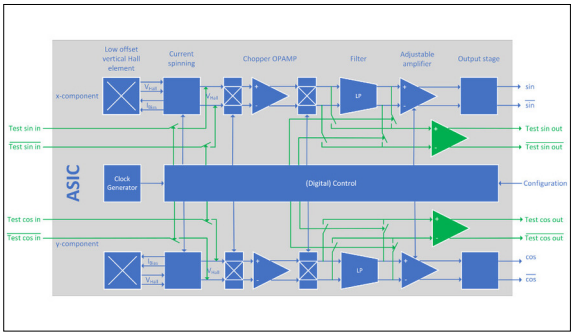

Figure 1: System Design with Test Structures
Own presentment

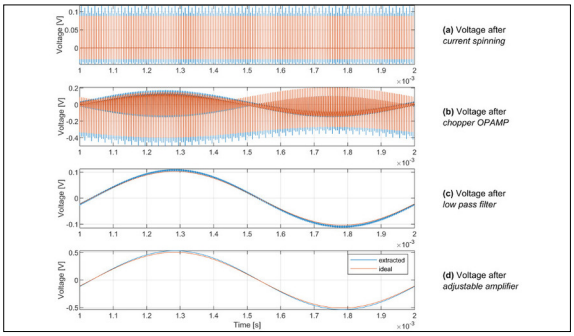

Figure 2: Simulation of extracted Layout
Own presentment

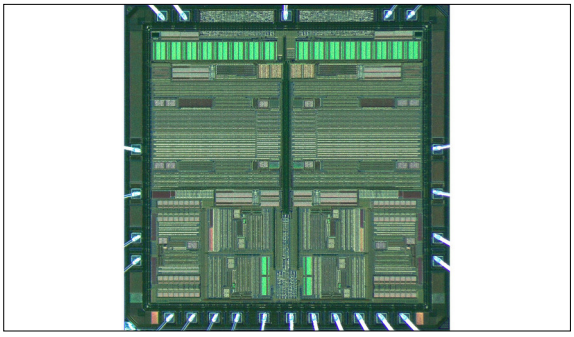

Figure 3: Photo of the developed ASIC
Own presentment

Introduction: The German company Dr. Fritz Faulhaber GmbH & Co. KG is specialized in miniature and micro motors and supplier of encoders with different resolutions, some of which are based on the magnetic principle. These encoders consist of three Hall elements which are directly integrated into the motors. Often, high precision is needed, which increases the costs accordingly, as the placement of the Hall elements is subject to strict tolerances.

The objective of this work is to develop a novel application-specific integrated circuit (ASIC). This ASIC should contain two vertical Hall elements and generate two differential signals, which have an offset of 90° relative to each other. Furthermore, the exact phase-shift and amplitude of these signals shall be freely configurable.

Approach: In the first phase, the CMOS design from the previous work was revised. Further, the two remaining digital blocks and the test infrastructure were planned and designed. Out of this design, the layout of the ASIC was created in a 600nm process from X-FAB. Special attention had to be paid in order to reach the size requirement of 3mm x 3mm for the whole chip. Two different vertical Hall elements with an expected sensitivity of 8.6µV / (mA mT) and 2.8µV / (mA mT), were as well developed and integrated. The correct functionality of the ASIC layout was checked by (corner)-simulations and compared with simulations of the CMOS design. Subsequently, in a second phase, the chip, which had been produced in the meantime, was tested and characterized. A fully automatic test procedure for measuring all individual blocks on the ASIC and the entire system was developed for this purpose.

Result: In the scope of this work, the frontend design was completed, and the layout of the ASIC was developed. The chip amplifies the measured Hall signals and reduces the offset voltages of the Hall elements up to a factor of 9. Additionally, the final amplification of the signals is configurable. The chip functions correctly over a temperature range of −40°C to 125°C and a voltage range of 2.5V to 5V. The integrated vertical Hall elements have a measured sensitivity of 7.5µV / (mA mT) and 2.3µV / (mA mT).