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Development of a Time-to-Digital Converter in SiGe-Technology

Development of a Gated Vernier Ring Oscillator based TDC in 130nm SiGe-Technology

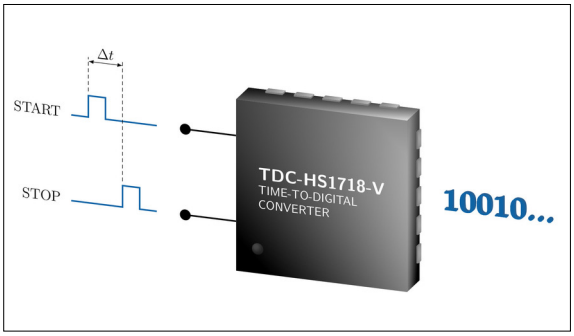
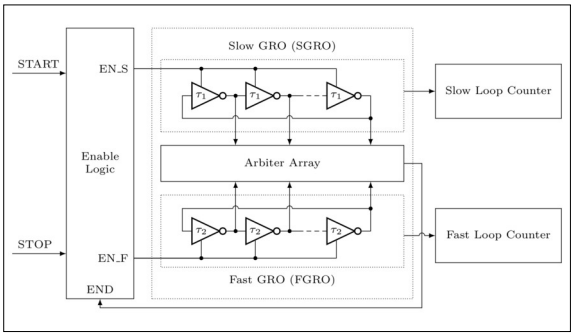
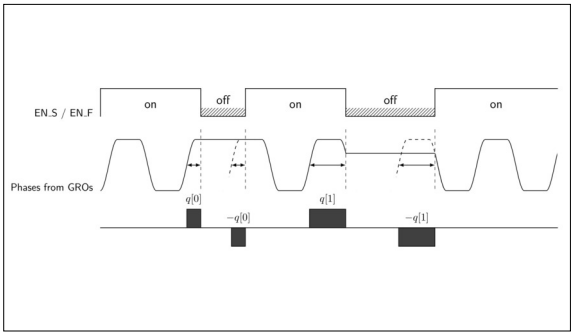


Illustration of the proposed TDC ASIC



Concept of the proposed TDC



Timing diagram of a gated ring oscillator

Introduction: None-contact distance measurement systems are increasingly used in industry and everyday life, for example in automotive vehicles.
The distance measurement by using time of flight of ultrasonic waves has been used for a long time. Using light waves is a method that has only become technically possible due to the ever faster electronic circuits. Today there are commercial time-to-digital converters which are able to measure a time differences of less than 50ps.
In this thesis, a time-to-digital converter should be designed for a future proprietary application-specific integrated circuit using IHPs 130nm silicon-germanium-technology, which will be able to measure even lower time differences.

Objective: To get into the topic of time-to-digital converter, this thesis starts with an explanation of different time-to-digital converter architectures. The literature research sheds light on recently published works and analyses the architectures used and performance parameters achieved.
A standard inverter in IHPs 130nm technology has a gate-delay of 36ps. To achieve the specified resolution of less than 10ps, an architecture with sub gate-delay is required. In the intended application, a measurement is performed several times. The architecture of the gated Vernier ring oscillator is predestined for such an application.
The development of the design started with the delay element for the gated ring oscillator. Further blocks were developed until the gate Vernier ring oscillator was set up. The detection circuit is very time-critical and requires a lot of attention. In order to build up a complete time-to-digital converter, additional components such as counters, a shift register or a padframe are required and developed.

Result: The design of the application-specific integrated circuit TDC-HS1718-V is developed from the inside out. The time-to-digital-converter is based on the Vernier principle and uses two gated ring oscillators on a slightly different frequency.
The gated ring oscillators are built on 37 stages. The delay per stage differs by approximately 2ps, which corresponds to the theoretical resolution. The resulting period are 1.44ns and 1.37ns with a coefficient of variance below 5%. The frequency of the slow gated ring oscillator can be easily adjusted via an external supply voltage, giving the design more flexibility.
The general functions of enabling the gated ring oscillators and disabling them depending on the measured time interval works as expected. The enable logic for the loop counters does not work in all conditions and must be modified.
Before starting the layout, a revision of the designed circuit is necessary. To determine the final resolution, simulations are required that include both the time-to-digital converter and the padframe.