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Time to Digital Converter

A Vernier Implementation on Field Programmable Gate Arrays

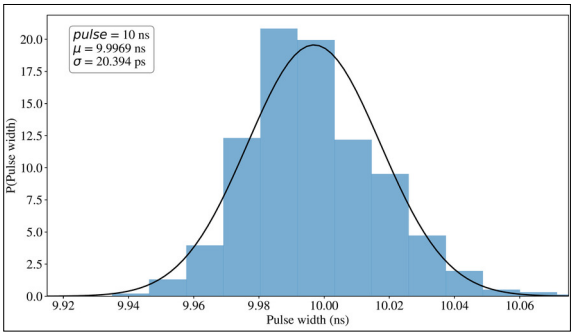

Figure 1: Probability density function of 10000 measured pulses on a low cost FPGA board
Own presentment

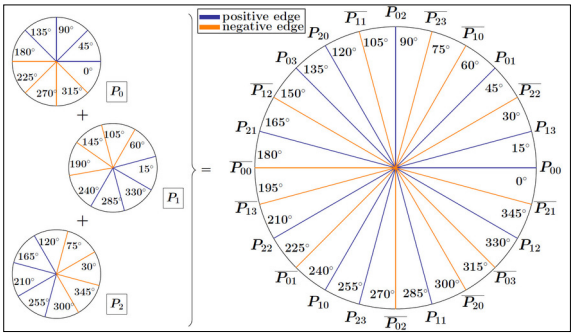

Figure 2: Shifted output clocks of the PLL instances to generate fine clock network
Own presentment, based on DOI: 10.1109/TVLSI.2019.2962606

Introduction: With the ongoing development in various scientific fields like nuclear physics, biomedical engineering and time-of-flight applications, the need to measure short time intervals and convert these into a digital format is higher than ever before. Time to Digital Converters (TDCs) are capable of measuring time intervals in the picosecond region. The Institute for Microelectronics and Embedded Systems has used Tapped Delay Line (TDL) TDCs successfully for many years. The downside of these TDLs is, that they rely heavily on constant delay times. For this thesis, new implementation methods should be evaluated and implemented. Special attention shall be paid to the Vernier principle.

Approach: In the literature study, the most appealing papers were summarized. In particular, two subsequent publications from the same research group caught our attention. The centerpiece of both is a counter matrix. One of them (Fig. 3, left) is based solely on the use of the Phase Locked Loop (PLL) hardware of the FPGA. These PLLs are phase shifting and overclocking the system clock in order to generate a discrete uniform distributed clock network (Fig. 2) for the counter matrix. The second one (Fig. 3, right) uses a hybrid structure that utilizes the PLL in combination with delay elements. Both variants were implemented as single-core and multi-core TDCs on several Xilinx FPGAs using VHDL.

Conclusion: The achieved standard deviation of the measured pulse width for the best possible implementation with a stochastic multi-core approach is as low as 13 ps. Even with an implementation on an inexpensive FPGA, good results can be achieved (Fig. 1).
The performance of the implemented TDCs is in the same range as reported in the publication mentioned above. However, a properly calibrated TDL TDC is superior regarding the standard deviation. Nevertheless, this thesis shows an easy to handle and reasonably powerful alternative.

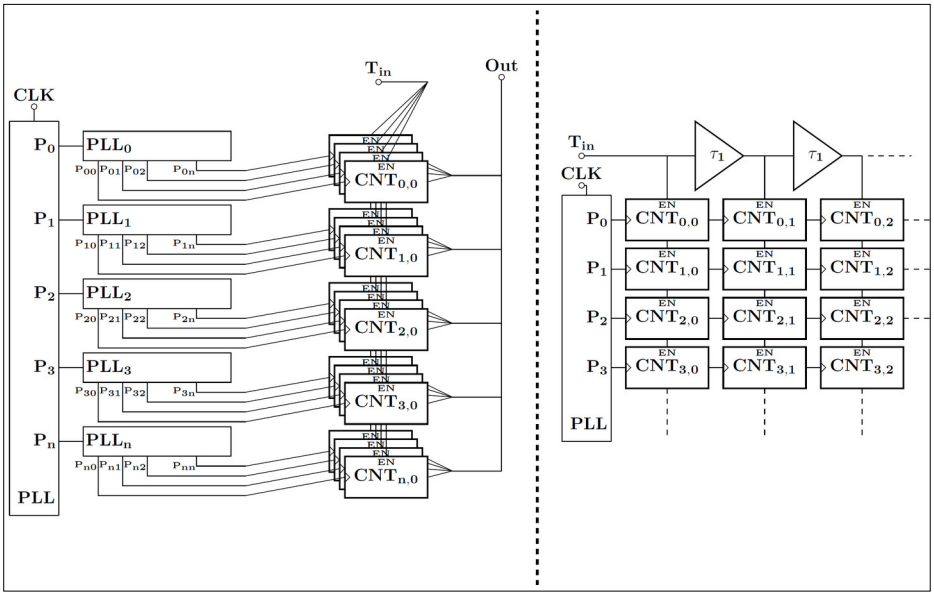

Figure 3: Theoretical schematics for measuring an input pulse (T_in) with a counter matrix
Own presentment, based on DOI: 10.1109/TVLSI.2016.2569626