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Subject Area	Sensor, Actuator and Communication Systems

Design of a Time-to-Digital Converter in 130 nm SiGe-Technology

Development, Layout and Post-Layout Simulations

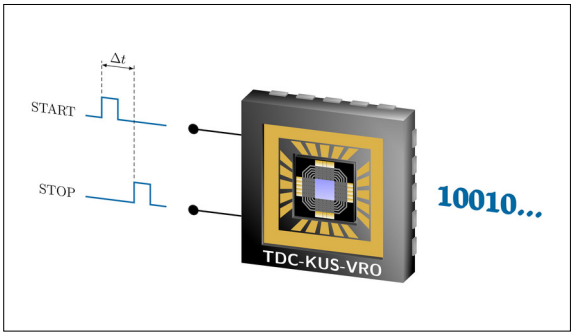
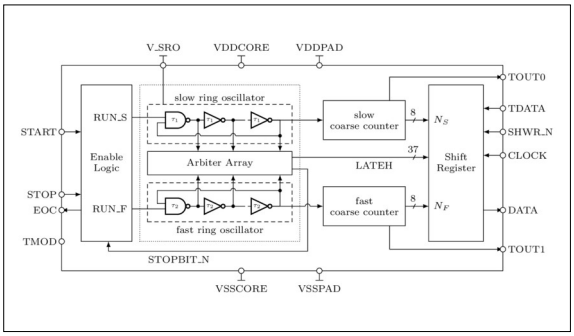
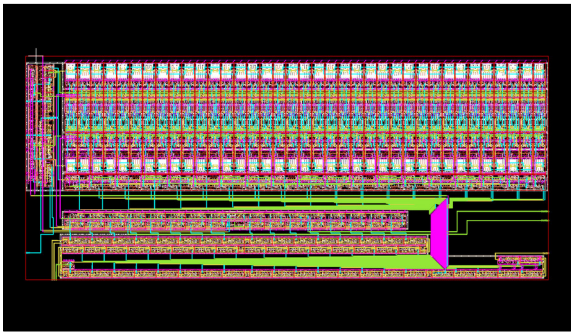


Illustration of the time-to-digital converter functionallity.



Block design of the implemented time-to-digital converter.



Layout of the implemented time-to-digital converter.

Introduction: Non-contact distance measurement systems are increasingly used in industry and everyday life, for example in automotive vehicles. The distance measurement using light waves is a method that has only become technically possible due to the ever faster electronic circuits. In a previous project, a time-to-digital converter has been developed on schematic level in an IHP 130 nm SiGe-technology. A multi-path Vernier gated ring oscillator architecture has been used to achieve a time resolution below 10 ps. However, the design is further improved and implemented. Post-layout simulations are taken into account to evaluate the achieved performance parameters and give further leads on possible improvements.

Objective: This master thesis starts with a comprehensive review and design improvements. Setting up the development environment as well as writing conversion scripts to handle the design data between the different tools is also part of this project. To achieve realistic simulation results, the parasitic effects are taken into account. The post-layout simulations use the layout information of the two ring oscillators and the comparison circuit to do so. The results show a doubling of the ring oscillators delay time, which is the result of the parasitic capacitance on the ring oscillator's internal nodes. The resulting delay is almost as slow as the delay of a single-path ring oscillator. The architecture choice needs to be reconsidered, taking into account the new findings because the parasitic effects erase the advantages of the implemented architecture. The re-evaluation of different architecture performance parameters result in changing the architecture to the single path Vernier ring oscillator architecture. Using a single-path structure reduces the parasitic capacitance on the internal ring oscillator node to about a third compared to the multi-path structure.

Result: The developed chip TDC-KUS-VRO has a built-in time-to-digital converter which works according to the Vernier principle to measure a time delay between two single subsequent events. The presented time-to-digital converter achieves a time resolution of 3 ps and has a maximal measurement range of 473 ps. The nominal ring oscillator period times are 2.2 ns and 2.1 ns. The oscillators consist of 37 stages which results in a delay per stage of 59 ps and 56 ps. The slow ring oscillator frequency is adjustable using a separate power supply. The active power consumption amounts to 9.8 mW on the 1.2 V core power supply and to 5.3 mW on the 3.3 V pad power supply. The signal pulse on the START input pin indicates the start and the signal pulse on the STOP input pin the end of the time interval to be measured. The coarse counters count the number of wraps of the ring oscillators. The Vernier principle evaluates the time after signal STOP until the ring oscillators are synchronized. As soon as the conversion is finished, the data are cached and ready to be read out of the 55 bit serial-out shift register. The presented time-to-digital converter performance parameters are simulated using the parasitic model of the time-to-digital converter core and the model of the pad cells. Due to the limitations of using the pre-release version of the process design kit with Tanner tools, the export of the pad cells is pending.