Dynamic Hardware Reconfiguration for Flexible Enhancements in Embedded Systems

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Introduction: This semester project examines the "QuickLogic EOS-S3 SoC", based on the "SparkFun QuickLogic Thing Plus - EOS S3" board, as a basis for a dynamically reconfigurable hardware system. The goals are to implement a prototype application demonstrating the eFPGA reconfiguration abilities of the EOS-S3 and, if the given time allows for it, to develop an application where a neural network too big to fit onto the eFPGA fabric at once is split into several stages and inferenced sequentially via reconfiguration.

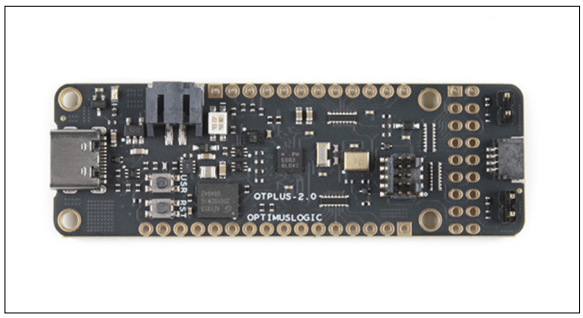
Approach: As a first step, the tooling surrounding the EOS-S3 needed to be examined. f4pga is the open source FPGA toolchain used to generate the bitstreams for the EOS-S3 from HDL source code. Because of several features lacking in the f4pga flow, a few of the tools used in the flow must be built from source, such as GHDL and Yosys, as well as modifying f4pga scripts to enable VHDL support.

The prototype application could not be implemented due to several hindrances, mostly stemming from severely lacking, contradictory or false documentation provided by the manufacturer. All attempts to contact QuickLogic have been left unanswered.

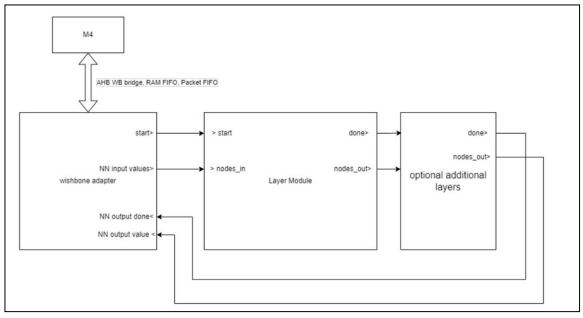
Some very basic ideas were gathered on how to approach an neural network implementation on an FPGA, namely splitting a neural network along its layers and transforming them into VHDL entities with a fixed interface. The interface would allow the M4 to retrieve inference results through the wishbone adapter module without software changes.

Result: The original goals of this semester project were unfortunately not achieved. However, knowledge about the inner workings of the f4pga open source ecosystem was gained and documented.

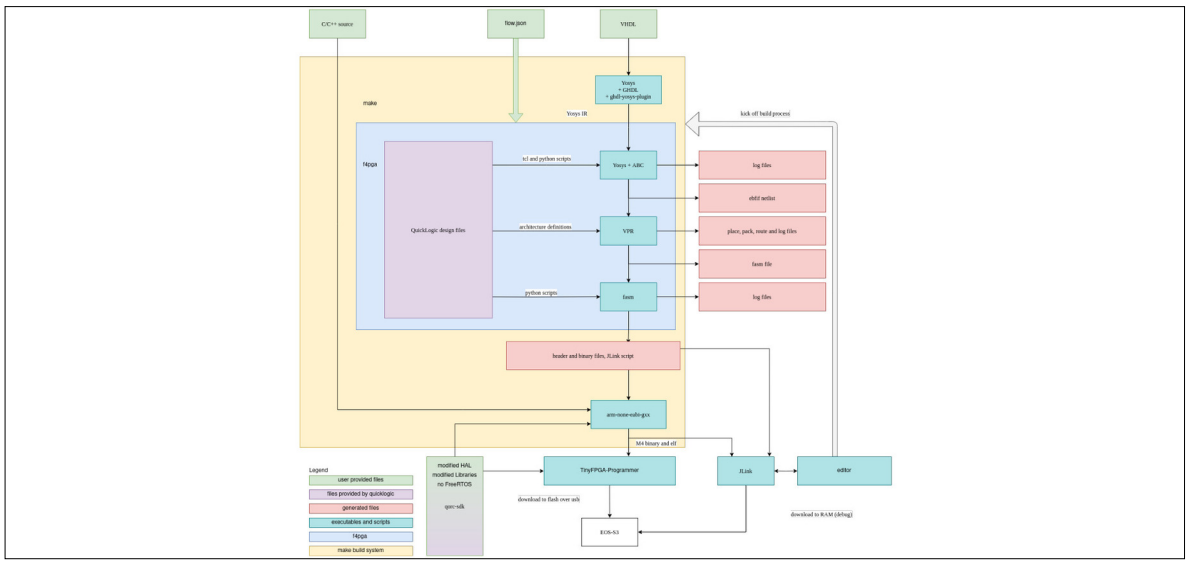
SparkFun QuickLogic Thing Plus - EOS S3
https://www.sparkfun.com/products/17273



Neural Network Layer Split
Own presentment



Tooling Flow
Own presentment



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Subject Area
Embedded Systems