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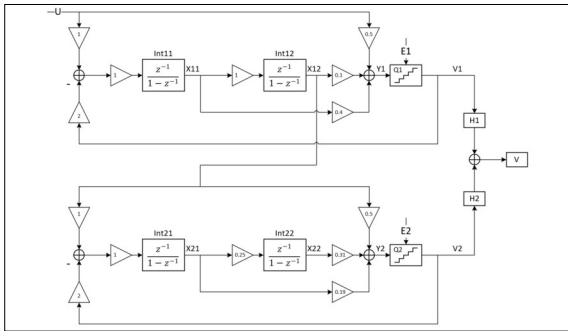
Florian Krischker



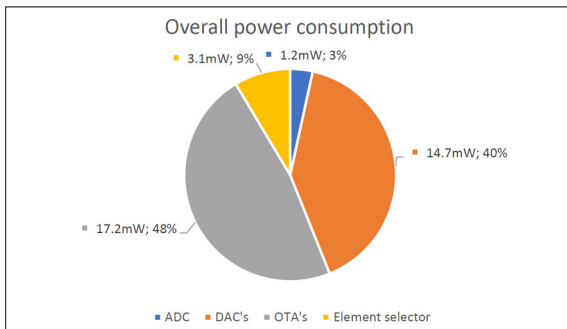
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Subject Area	Sensor, Actuator and Communication Systems

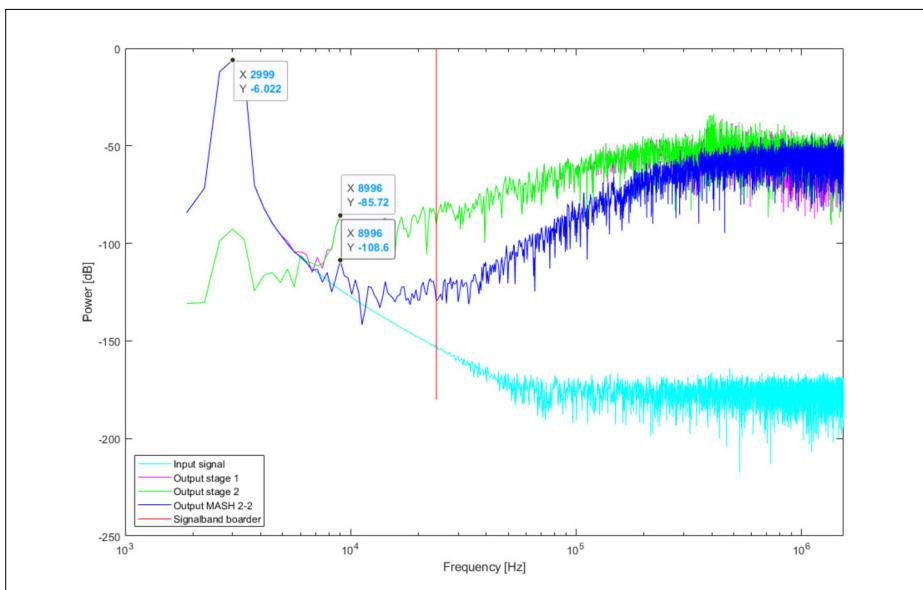
Development of a Delta Sigma modulator for audio applications



Proposed MASH 2-2 structure
Own presentment



Overall powerusage of the proposed circuit
Own presentment



Powerspectrum of input and output signals
Own presentment

Introduction: Delta-Sigma-Modulators are the first choice when signals up to a bandwidth of 1 MHz have to be digitized with high resolution. This is often the case in areas where environmental parameters and sound must be converted. The main operating principle of this family of analog-to-digital converters is oversampling and noise shaping, which results in their high resolution.

Approach: The focus of this work is the development of a 16-bit delta-sigma modulator, which has at least a system order of two and uses a multibit approach. In a first phase different system topologies are compared against each other. In a second phase a system with a selected topology is designed and implemented in a 350 nanometer CMOS process.

Result: A two-stage multi-stage noise shaping (MASH) delta-sigma modulator with a 2-bit quantizer in the first stage and a 3-bit quantizer in the second stage was proposed to achieve fourth order noise shaping. A Silva Steensgaard structure was chosen as the structure for the two stages. The modulator has a differential configuration and is designed in discrete-time with switched capacitor components. The integrators are based on folded cascode operational transconductance amplifiers. While the implemented digital-to-analog converters are capacitive with a rotary element selector to reduce mismatch. The internally used analog-to-digital converter is a Strongarm comparator with differential input. The proposed MASH 2-2 structure achieves a signal-to-quantization-noise ratio (SQNR) of 102dB for a half-scale differential input signal at nominal simulation setting. This corresponds to an SQNR of 108dB for a full-scale input signal. The circuit has a signal-to-noise ratio of 98dB when considering thermal noise. This corresponds to an achieved effective number of bits (ENOB) of 16. In normal operation the MASH 2-2 structure consumes about 36 milliwatts of power. At an achieved bandwidth of 24 kilohertz, this results in a Schreiers figure of merit of 156dB.